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EXAMINER	
NORTON, JENNIFER L	
ART UNIT	**PAPER NUMBER**
2121	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/710,065	DENTON ET AL.	
	Examiner	Art Unit	
	Jennifer L. Norton	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The following is a **Final Office Action** in response to the Amendment received on 12 April 2007. Claims 5, 7, 8, 10-12 and 16 been amended. Claims 1-35 are pending in this application.

Drawings

2. The amendment to the Drawings was received on 12 April 2007. The correction is acceptable and the objection is withdrawn.

Specification

3. The amendment to the Specification was received on 12 April 2007. The correction is acceptable and the objection is withdrawn.

Claim Rejections - 35 USC § 112

4. The amendment to the Claims was received on 12 April 2007. The correction is acceptable and the rejection is withdrawn.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claim 1 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The optimization of the floor schedule based on sensitivity data in the disclosed application, given its broadest reasonable interpretation consistent with the specification, is considered to include mathematical algorithms that have not been incorporated in any computer readable medium to produce a useful, concrete and tangible result. Claim 1 appears to be directed to an abstract idea and process of optimization of a floor schedule rather than a practical application of the process.

7. Claims 2-6 are rejected under 35 U.S.C 101 since they depend from claim 1 and do not correct the deficiency of claim 1.

8. Claims 12-18 are rejected under 35 U.S.C. 101. Claim 12, lines 1-2, the phrase "computer usable medium" has not been defined in the specification. Accordingly, when this phrase is given its broadest reasonable interpretation consistent with the specifications, "medium" is considered to include transitory waves and carrier waves. Such waves are not considered to be patentable subject matter, see O'Reilly v. Morse, 56 U.S. (15 How) 62 (1854).

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1, 2, 4, 7-10, 12-16, 18-21, 23, 24, 26, 27 and 29-31 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,842,661 (hereinafter Chong).

11. As per claim 1, Chong discloses a method comprising the steps of:

a. providing a floor schedule (Fig. 9, element 940) of an assembly unit (Fig. 9) for a device (col. 7, lines 29-35 and 59-67, col. 8, lines 26-32 and Fig. 9, element 910a and 910b); and

b. optimizing the floor schedule based on sensitivity data (col. 5, lines 10-26, col. 8, lines 48-52 and col. 9, lines 27-33) of the device (col. 10, lines 6-13) during operation of the assembly unit on the floor schedule (col. 5, lines 33-36 and col. 9, lines 27-41).

12. As per claim 2, Chong discloses the steps of receiving the sensitivity data and optimizing the floor schedule in real-time (col. 9, lines 27-41).

13. As per claim 4, Chong discloses the steps of generating sensitivity data for the device of an assembly unit during operation of the assembly unit on a floor schedule (col. 5, lines 10-14); and

receiving an optimal path data of the floor schedule based on the sensitivity data (col. 9, lines 4-8),

wherein the optimal path data controls the path of the device through the assembly unit (col. 10, lines 6-13 and 18-22).

14. As per claim 7, Chong discloses step b) further comprises a step of analyzing the sensitivity data of the device to estimate an amount of sensitivity of the device (col. 5, lines 10-23).

15. As per claim 8, Chong discloses step b) further comprises a step of analyzing the sensitivity data through at least one sensitivity model (i.e. predetermined electrical values for particular interconnect locations) to estimate an amount of sensitivity of the device (col. 5, lines 10-23).

16. As per claim 9, Chong discloses the sensitivity model includes a machine model (col. 5, lines 17-25 and 59-64; i.e. predetermined electrical values for particular interconnect locations).

17. As per claim 10, Chong discloses a step of estimating a result of the at least one sensitivity model with a second sensitivity model (Fig. 9, element 950) in the case that data of the at least one sensitivity model is incomplete (col. 8, lines 39-52).

18. As per claim 12, Chong discloses a tangible computer program product (col. 8, lines 19-21 and col. 10, lines 36-42) comprising a computer useable medium (Fig. 9, element 932) having computer readable program code embodied therein for optimizing a floor schedule of an assembly unit for a device (col. 5, lines 33-36 and col. 9, lines 27-41), the program product comprising:

program code configured to analyze sensitivity data for the device during operation of the assembly unit on the floor schedule (col. 5, lines 33-36 and col. 9, lines 27-41); and

program code configured to optimize the floor schedule of the assembly unit based on the sensitivity data (col. 5, lines 10-26, col. 8, lines 48-52 and col. 9, lines 27-33).

19. As per claim 13, Chong discloses program code configured to generate the sensitivity data for the device being assembled by the assembly unit (col. 5, lines 10-15 and col. 8, lines 48-52).

20. As per claim 14, Chong discloses the analyzing program code analyzes the sensitivity data through at least one sensitivity model (i.e. predetermined electrical values for particular interconnect locations) to estimate an amount of sensitivity of the device (col. 5, lines 10-23).

21. As per claim 15, Chong discloses the sensitivity model includes a machine model (col. 5, lines 17-25 and 59-64; i.e. predetermined electrical values for particular interconnect locations).

22. As per claim 16, Chong discloses the analyzing program code further estimates a result of the at least one sensitivity model (Fig. 9, element 950) with a second sensitivity model in response to that data of the at least one sensitivity model is incomplete (col. 8, lines 39-52).

23. As per claim 18, Chong discloses the sensitivity data is received through a messaging system from at least one of the assembly unit and a testing unit (col. 5, lines 37-49 and col. 10, lines 36-42).

24. As per claim 19, Chong discloses an optimizer system comprising:

a model analyzer (Fig. 3, element 360) for receiving sensitivity data for a device of an assembly unit (col. 7, lines 25-29), and analyzing the sensitivity data during operation of the assembly unit on a floor schedule (col. 7, lines 29-35); and

a scheduling optimizer (Fig. 8, element 830) for optimizing the floor schedule of the assembly unit based on the analyzed sensitivity data (col. 7, lines 47-58 and col. 9, lines 27-33).

25. As per claim 20, Chong discloses a testing unit (Fig. 3, element 330) for generating sensitivity data for the device (col. 5, lines 10-14).

26. As per claim 21, Chong discloses the sensitivity data is received through a messaging system from at least one of the assembly unit and the testing unit (col. 5, lines 37-49 and col. 10, lines 36-42).

27. As per claim 23, Chong discloses wherein the sensitivity data is generated through at least one sensitivity model (col. 5, lines 17-25).

28. As per claim 24, Chong discloses the sensitivity model includes a machine model (col. 5, lines 17-25 and 59-64; i.e. predetermined electrical values for particular interconnect locations).

29. As per claim 26, Chong discloses a method comprising the steps of:

generating sensitivity data (col. 5, lines 10-26 and col. 8, lines 48-52) for a device (col. 8, lines 32-40 and Fig. 9, element 910a and 910b) of an assembly unit during operation of the assembly unit on a floor schedule (col. 4, lines 60-63 and col. 5, lines 10-14); and

receiving an optimal path data of the floor schedule that is generated based on the sensitivity data (col. 9, lines 4-8),

wherein the optimal path data controls the path of the device through the assembly unit (col. 10, lines 6-13 and 18-22).

30. As per claim 27, Chong discloses the steps of generating the sensitivity data and receiving the optimal path data in real-time (col. 9, lines 27-41).

31. As per claim 29, Chong discloses the sensitivity data is transmitted through a messaging system (col. 5, lines 37-49 and col. 10, lines 36-42).

32. As per claim 30, Chong discloses the generating step further comprises the step of generating at least one sensitivity model with the sensitivity data (col. 5, lines 17-25 and 59-64).

33. As per claim 31, Chong discloses the sensitivity model includes a machine model (col. 5, lines 17-25 and 59-64; i.e. predetermined electrical values for particular interconnect locations).

Claim Rejections - 35 USC § 103

34. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

35. Claims 3 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong in view of U.S Patent Publication No. 2004/0082083 (hereinafter Kraz).

36. As per claim 3, Chong teaches to measuring electrical characteristics of devices formed across the semiconductors used to quantify the performance of the processing tools (col. 8, lines 48-52 and 55-58).

Chong does not expressly teach the sensitivity data includes at least one of electrostatic discharge sensitivity data, electrical overstress sensitivity data, latch-up data, hot electron data, mobile ion contamination data, and negative bias threshold instability data.

Kraz teaches to measuring and monitoring electrostatic discharge and electrostatic voltage for a process tool (pg. 2, par. [0009], pg. 3, par. [0025], pg. 3-4, par. [0031]-[0032] and Fig. 2, element 20).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Chong to include measuring and monitoring electrostatic discharge and electrostatic voltage for a process tool to provide the automatic detection and response to an ESD event, in addition to providing advanced filtering of irrelevant ESD occurrences (including electrostatic discharge or electrostatic voltage) and the collection of valuable statistics on ESD environment for failure analysis and as evidence of compliance with customer's ESD requirements (pg. 3, par. [0028]).

37. As per claim 28, Chong teaches to measuring electrical characteristics of devices formed across the semiconductors used to quantify the performance of the processing tools (col. 8, lines 48-52 and 55-58).

Chong does not expressly teach the sensitivity data includes at least one of electrostatic discharge sensitivity data, electrical overstress sensitivity data, latch-up data, hot electron data, mobile ion contamination data, and negative bias threshold instability data.

Kraz teaches to measuring and monitoring electrostatic discharge and electrostatic voltage for a process tool (pg. 2, par. [0009], pg. 3, par. [0025], pg. 3-4, par. [0031]-[0032] and Fig. 2, element 20).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Chong to include measuring and monitoring electrostatic discharge and electrostatic voltage for a process tool to provide the automatic detection and response to an ESD event, in addition to providing advanced filtering of irrelevant ESD occurrences (including electrostatic discharge or electrostatic voltage) and the collection of valuable statistics on ESD environment for failure analysis and as evidence of compliance with customer's ESD requirements (pg. 3, par. [0028]).

38. Claims 11, 22 and 32-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong in view U.S. Patent No. 6,535,783 (hereinafter Miller).

39. As per claim 11, Chong does not expressly teach wherein step b) further comprises a steps of inhibiting a failed tool of the assembly unit based on the sensitivity data; and optimizing the floor schedule to avoid the failed tool.

Miller teaches to inhibiting a failed tool of the assembly unit based on the data (col. 5, lines 58-62 and col. 6, lines 42-45); and optimizing the floor schedule to avoid the failed tool (col. 5, lines 62-67 and col. 6, lines 35-38).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Chong to include to inhibiting a failed tool of the assembly unit based on the data; and optimizing the floor schedule to avoid the failed tool to prevent the further production of faulty wafers by the tool (col. 7, lines 52-56).

40. As per claim 22, Chong teaches the testing unit further comprises a sensitivity monitor (Fig. 3, element 330) for generating sensitivity data (col. 5, lines 10-14);

a reliability generator (Fig. 3, element 310) for generating reliability data having rules for the device and assembly unit (col. 5, lines 17-25 and 59-64; i.e. predetermined electrical values for particular interconnect locations); and

a tool controller (Fig. 3, element 350) for invoking the sensitivity monitor and reliability generator (col. 5, lines 17-23).

Chong does not expressly teach shutting down a testing tool of the testing unit.

Miller teaches shutting down a tool (col. 5, lines 58-62 and col. 6, lines 42-45).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Chong to include shutting down a testing tool of the testing unit to prevent the further production of faulty wafers by the tool (col. 7, lines 52-56).

41. As per claim 32, Chong teaches a testing unit comprising:

a sensitivity monitor (Fig. 3, element 330) for generating sensitivity data for a device (col. 5, lines 10-14);

a reliability generator (Fig. 3, element 310) for generating reliability data having rules for the device (col. 5, lines 17-25 and 59-64; i.e. predetermined electrical values for particular interconnect locations); and

a tool controller (Fig. 3, element 350) for invoking the sensitivity monitor and reliability generator (col. 5, lines 17-23).

Chong does not expressly teach shutting down a testing tool of the testing unit (col. 5, lines 58-62 and col. 6, lines 42-45).

Miller teaches shutting down a tool (col. 5, lines 58-62 and col. 6, lines 42-45).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Chong to include shutting

down a testing tool of the testing unit to prevent the further production of faulty wafers by the tool (col. 7, lines 52-56).

42. As per claim 33, Chong teaches as set forth above a messaging system (col. 5, lines 37-49 and col. 10, lines 36-42) for transmitting the sensitivity data and reliability data in real-time (col. 9, lines 27-41).

43. As per claim 34, Chong teaches as set forth above at least one sensitivity model is generated with the sensitivity data (col. 5, lines 17-25 and 59-64; i.e. predetermined electrical values for particular interconnect locations).

44. As per claim 35, Chong teaches as set forth above the sensitivity model includes a machine model (col. 5, lines 17-25 and 59-64; i.e. predetermined electrical values for particular interconnect locations).

45. Claims 5 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong in view of U.S. Patent No. 6,711,450 (hereinafter Conboy).

46. As per claim 5, Chong teaches step b) further comprises a step of testing of the device for sensitivities (col. 5, lines 10-14).

Chong does not expressly teach to prioritizing a testing of the device.

Conboy teaches to prioritizing the processing of a device (col. 6, lines 13-22).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Chong to include prioritizing the processing of a device to provide more flexibility in responding to changes in conditions (col. 5, lines 32-37).

47. As per claim 17, Chong teaches the optimizing program code tests the device for sensitivities (col. 5, lines 10-14).

Chong does not expressly teach to the optimizing program code prioritizes a testing of the device.

Conboy teaches to prioritizing the processing of a device (col. 6, lines 13-22).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Chong to include prioritizing the processing of a device to provide more flexibility in responding to changes in conditions (col. 5, lines 32-37).

48. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chong in view of Conboy in further view of U.S. Patent No. 6,351,684 (hereinafter Shirley).

49. As per claim 6, Chong in view of Conboy does not expressly teach the prioritizing step includes prioritizing the testing of a mask based on a size of a space on the mask.

Shirley teaches to testing a mask based on characteristics of a mask (col. 4, lines 54-67, col. 5, line 67 and col. 6, lines 1-17).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Chong in view of Conboy to include testing a mask based on characteristics of a mask to reduce wafer processing cycle time by knowing the exact location of the mask, providing flexibility of re-routing certain masks to the processing of more critical wafer lots due to business judgment rule, quality issue that has surfaced (col. 3, lines 24-29).

50. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chong in view of Miller in further view of Conboy.

51. As per claim 25, Chong in view of Miller as set forth above teaches the scheduling optimizer further comprises:

optimizing the floor schedule in real-time (col. 9, lines 27-41) based on the sensitivity data and the reliability data (col. 5, lines 10-26, col. 8, lines 48-52 and col. 9, lines 27-33).

Chong in view of Miller does not expressly teach automated material handling system dispatcher and a maintenance scheduler for scheduling maintenance based on the sensitivity data and the reliability data.

Conboy teaches to an automated material handling system dispatcher (col. 4, lines 3-11) and a maintenance scheduler for scheduling maintenance (col. 6, lines 62-67 and 8, lines 9-12).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Chong in view of Miller to include an automated material handling system dispatcher and a maintenance scheduler for scheduling maintenance to provide more flexibility in responding to changes in conditions (col. 5, lines 32-37).

Response to Arguments

52. Applicant's arguments see Remarks pgs. 12-13, filed 12 April 2007 with respect to claims 12-18 under 35 U.S.C. 101 have been fully considered but they are not persuasive.

53. As per claim 1, Applicant has not incorporated the method of optimization of the floor schedule in any computer readable medium to produce a useful, concrete and tangible result. Thus, Claim 1, as well as claims 2-6 dependent therefrom, stand rejected under 35 U.S.C. 101.

54. As per claims 12-18, the Applicant asserts that carrier waves can be tangible, hence "statutory articles"; the Examiner respectfully disagrees. The Examiner reiterates, as set forth above and in the Non-Final Office Action mailed on 12 January 2006, carrier waves are **not** statutory; hence such waves are not considered to be patentable subject matter, see O'Reilly v. Morse, 56 U.S. (15 How) 62 (1854).

Therefore, the rejection of claims 12-18 stand rejected as set forth above based on Applicant's assertion that tangible carrier waves are statutory articles, which encompass the scope of Applicant's invention.

55. Applicant's arguments see Remarks pgs. 13-14, filed 12 April 2007 with respect to claims 1, 2, 4, 7-10, 12-16, 18-21, 23, 24, 26, 27 and 29-31 under 35 U.S.C. 102 (e) have been fully considered but they are not persuasive.

56. Applicant argues that the prior art fails to teach, ""optimizing the floor schedule based on sensitivity of data of the device" (Claim 1, similarly claimed in claims 12,19 and 26)", the examiner respectfully disagrees.

57. The Applicant discloses, (pg. 2, par. [0033]) "sensitivity data of the device (e.g., ESD sensitivity data, or similar data involving risk factors of the device)".

Chong discloses (col. 5, lines 10-26) "The system 300 also comprises a wafer electrical test (WET) unit 330 that is capable of performing a plurality of electrical tests that provide data relating to the electrical characteristics of various interconnect locations (e.g., contacts and/or vias) on the semiconductor wafers 105. The system 300 may comprise a plurality of sub-controllers 350 that are capable of controlling various process steps that are performed on the semiconductor wafers 105. For example, the process controller 310 may provide predetermined electrical characteristic values, such as a predetermined resistivity value for particular interconnect locations, which may be used by the sub-controllers 350 to calculate control adjustments for various control process steps performed on the semiconductor

wafers 105. A more detailed illustration and description of the sub-controllers 350 is provided in FIG. 4 and accompanying description below."

(col. 8, lines 48-52) "The metrology data analysis unit 960 may collect, organize, and analyze data from the metrology tool 950. The metrology data is directed to a variety of physical or electrical characteristics of the devices formed across the semiconductor wafers 105."

(col. 9, lines 27-33) "Upon analysis of the metrology data and/or the WET data, the system 300 may implement an interconnect characteristic control process to affect the characteristics of interconnect locations (e.g., vias, contact, etc.) on the semiconductor wafers 105 (block 1060). Feedback and/or feed forward corrections may be utilized to control interconnect characteristics formed on the semiconductor wafers 105."

Chong discloses sensitivity data as "data involving risk factors of the device" (i.e. electrical characteristics) as defined by the Applicant. Furthermore, Chong meets the claimed limitation "optimizing the floor schedule based on sensitivity of data of the device", (i.e. feedback or feedforward corrections).

58. Applicant's arguments see Remarks pgs. 14-15, filed 12 April 2007 with respect to claims 3, 5, 6, 11, 17, 22, 25, 28 and 32-35 under 35 U.S.C. 103 (a) have been fully considered but they are not persuasive.

59. Applicant argues that the prior art fails to teach, "generating sensitivity data for a device", the examiner respectfully disagrees.

60. The Applicant discloses, (pg. 2, par. [0033]) "sensitivity data of the device (e.g., ESD sensitivity data, or similar data involving risk factors of the device)".

Chong discloses (col. 5, lines 10-26) "The system 300 also comprises a wafer electrical test (WET) unit 330 that is capable of performing a plurality of electrical tests that provide data relating to the electrical characteristics of various interconnect locations (e.g., contacts and/or vias) on the semiconductor wafers 105."

Hence, Chong discloses sensitivity data as "data involving risk factors of the device" (i.e. electrical characteristics) as defined by the Applicant.

61. Claims 3, 5, 6, 11, 17, 22, 25, 28 and 32-35 stand rejected under 35 U.S.C 103 (a) as set forth above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following references are cited to further show the state of the art with respect to monitoring process and tools of a manufacturing system.

U.S. Patent No. 7,206,653 discloses a computer-implemented wafer-based planning methods for batch-based processing tools.

U.S. Patent No. 7,209,798 discloses a method for etch processing that allows the bias between isolated and nested structures/features to be adjusted, correcting for a process wherein the isolated structures/features need to be smaller than the nested structures/features and wherein the nested structures/features need to be reduced relative to the isolated structures/features, while allowing for the critical control of trimming.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer L. Norton whose telephone number is 571-272-3694. The examiner can normally be reached on 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anthony Knight can be reached on 571-272-3687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO

Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Anthony Knight
Supervisory Patent Examiner
Art Unit 2121